#13 Suppl Amdt KJ 8/30/02

EXPEDITED PROCEDURE - EXAMINING GROUP 2829

S/N 09/785,006 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Aaron M. Schoenfeld	Examiner:	Evan T Pert
Serial No.:	09/785,006	Group Art Unit:	2829
Filed:	February 16, 2001	Docket:	303.259US3
Title:	GRINDING TECHNIQUE FOR INTEGRATED CIRCUITS		

SUPPLEMENTAL AMENDMENT & RESPONSE UNDER 37 CFR 1.116

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Commissioner for Patents
Washington, D.C. 20231

In response to the Final Office Action mailed April 25, 2002 and the advisory action mailed July17, 2002, please amend the application as follows:

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect amendment of previously pending claims 11, 12, 14-18, 21-25, 35, 36 and 38-41. The specific amendments to claims 11, 12, 14-18, 21-25, 35, 36 and 38-41 are detailed in the following marked up claims.

11. (Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more planar perimeter side surfaces, each planar perimeter side surface extending between the first planar surface and the second planar surface;

a layer of scribe material forming the planar perimeter side surfaces, the layer of scribe material surrounding the circuitry; and

[at least a portion of at least one] each planar perimeter side surface of the semiconductor die having a [substantially flat, smooth] ground or polished surface.